REMARKS

Claims 1-22 are pending. No new subject matter has been added. Reconsideration is requested.

Claim Rejections – 35 U.S.C. § 102

Claims 1-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Dworkin et al., (US Pub. 2003/0058893). The limitations of claim 3 have been added to claim 1. Claim 1 now recites: *a processing circuit to receive synchronization pulses and receive a predicted master timestamp value associated with a future synchronization pulse, wherein the processing circuit receives the predicted master timestamp value asynchronously in Internet Protocol (IP) packets received over an IP connection.*

With respect to previous claim 3, the Examiner states that Dworkin at paragraph 38 discloses receiving the predicted master timestamp value asynchronously in Internet Protocol (IP) packets over an IP connection.

Dworkin at paragraph 38 does not suggest *receiving the predicted master timestamp value asynchronously in Internet Protocol (IP) packets over an IP connection.* Paragraph 38 only describes how voice and video servers are provided on a bi-directional transfer of Internet Protocol (IP) traffic between a cable system headend 102 and a plurality of cable modems 106 and 108 over a hybrid fiber-coaxial (HFC) cable network 110.

Conversely, Dworkin describes at paragraph 41 that master CMTS device 104A, slave CMTS device 104B and 104C, and calibration pulse generator 103 are connected to one another by a synchronization bus 112. The term synchronization bus is defined in paragraph 41 as PCI interface, back-plane bus, four-wire interface, coaxial able, or wireless path. There is no suggestion in Dworkin that the predicted master timestamp value is received asynchronously in Internet Protocol (IP) packets over an IP connection. FIG. 1 of Dworkin also shows a synchronization bus 112 connecting all of the CMTS devices 104 together within the headend 102 and does not suggest Internet Protocol (IP) packets sent over an IP connection as specified in claim 1.

One problem with using a backplane bus architecture as described in Dworkin is that additional interfaces have to be provided and dedicated to transporting synchronization information (see synchronization bus 112 in FIG. 1). Further, the CMTS devices may be

physically spaced apart and in different racks that would be problematic connecting together with backplane bus 112 of Dworkin.

Claim 1 uses an IP connection to send the IP master time clock to slave synchronization circuits in different CMTS devices. This eliminates many of the synchronization bus 112 connections required in Dworkin and increases scalability by increasing the number of CMTS' that can be synchronized and allows the CMTS' to be placed in a wider variety of locations.

Claim 3 has been amended to specify the Internet Protocol (IP) packets containing the master timestamp value as using multicast addresses. This is clearly described in the specification at page 4 lines 10-12. Using IP packets to carry the master timestamp value in combination with multicasting the IP packets further reduce the amount of bandwidth required to send the master timestamp to the slave CMTS' and at the same time increases scalability of the CMTS devices at the cable network headend.

Claim 10 describes how a *master* synchronization circuit predicts both a future synchronization pulse and then calculates a further master timestamp value that corresponds to the predicted future synchronization pulse. Claim 10 includes the element: *determine a difference between the first and second master timestamp values and an amount of time occurring between the first and second synchronization pulses.*

The examiner states that this is described as item 306 in FIG. 3 and in paragraph 72. However, paragraph 72 states that the compare circuit 306 only issues an internal pulse when two input values 305 and 315 are equal. Thus, Dworkin has no way to determine the *difference between the first and second master timestamp values and an amount of time occurring between the first and second synchronization pulses* as specified in claim 10.

The examiner further states that Dworkin as paragraph 83 calculates a future master timestamp value (TGC counter values) that corresponds to the future synchronization pulse by adding the second master timestamp value and the difference multiplied by the predetermined amount.

However, Dworkin at paragraph 83 only discusses how the master CMTS device 104 determines the FTSV values for each respective slave. There is no suggestion of the master

CMTS device predicting the occurrence of a future synchronization *pulse* according to the amount of time occurring between the first and second synchronization pulses and calculating a future master timestamp value that corresponds to the future synchronization pulse according to the difference between the first and second master timestamp values.

Claim 7 recites identifying an error condition according to a number of times the local timestamp counter is synchronized with received timestamp values. Claim 11 describes handing over the master synchronization circuit duties to a different slave synchronization circuit when the difference between the actual master timestamp value and the future master timestamp value is not within a predetermined range.

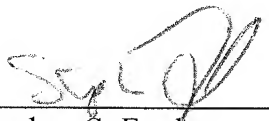
The examiner cites paragraphs 85 and 86 in Dworkin for disclosing these elements. However, paragraph 85 describes how new TGCCount (new) values are determined upon being reset. There is no suggestion that the slave CMTS 104B takes over the operations of a master CMTS. Paragraph 86 describes how latency is measured and never discloses a master synchronization circuit sending *an error message to the slave synchronization circuit when the difference between the actual master timestamp value and the future master timestamp value is not within a predetermined range that causes the slave synchronization circuit to take over operations as the master synchronization circuit* as specified in claim 11.

Accordingly, claims 1, 3, 10 and 11 are patentable under 35 U.S.C. 102(e) over Dworkin. The other independent and dependant claims have limitations similar to one of claims 1, 3, 10 or 11 and are therefore patentable over Dworkin for the same reasons.

For the foregoing reasons, reconsideration and allowance of claims 1-22 of the application as amended is requested. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

MARGER JOHNSON & McCOLLOM, P.C.



Stephen S. Ford
Reg. No. 35,139

MARGER JOHNSON & McCOLLOM, P.C.
210 SW Morrison Street, Suite 400
Portland, OR 97204
503-222-3613

Customer No. 20575